What is claimed is:

1. A multilayer board, comprising

a signal line requiring tamper-resistance, the signal line including: (a) a conductive trace and (b) a conductive via that passes through layers of the multilayer board, wherein

the conductive trace and an end of the conductive via existing on an outside layer of the multilayer board are placed under one or more circuit components mounted on the outside layer.

2. The multilayer board of Claim 1, wherein

the signal line further includes a conductive trace on an inner layer that is sandwiched between sheets of foil and/or circuit components placed on layers above and below the inner layer so that the sheets of foil and/or circuit components hide the conductive trace on the inner layer when viewed from above or below.

3. The multilayer board of Claim 2, wherein

the sheets of foil placed on the layers that are outside the inner layer are connected to either a ground or a power source.

4. The multilayer board of Claim 3, wherein

the conductive trace on the outside layer is further covered by a circuit component on another outside layer when viewed from above or below.

5. The multilayer board of Claim 2, wherein

the signal line requiring tamper-resistance is either a signal line that is input to an encryption unit or a signal line that is output from a decryption unit.

6. A multilayer board, comprising:

a certain signal line that includes (a) a conductive trace and (b) a conductive via that passes through layers of the multilayer board, wherein

the conductive trace and an end of the conductive via existing on an outside layer of the multilayer board are placed under one or more circuit components mounted on the outside layer,

the certain signal line further includes a conductive trace on an inner layer that is sandwiched between sheets of foil and/or circuit components placed on layers above and below the inner layer so that the sheets of foil and/or circuit components hide the conductive trace on the inner layer when viewed from above or below, and

the certain signal line is either a data line or an address

line.

7. A design apparatus for a multilayer board, the design apparatus comprising:

a component information acquiring means for acquiring component information that shows (a) positions of circuit components, (b) sizes of the components, and (c) terminals contained by the components;

a tamper-resistant signal line specifying means for specifying a signal line that requires tamper-resistance, among signal lines connecting terminals;

an outside layer wiring setting means for referring to the component information and setting areas on outside layers covered by circuit components as outside layer wiring possible areas;

a via setting means for referring to the component information, detecting an area where a first outside area wiring possible area of one outside layer overlaps another outside area wiring possible area of a second outside layer that is opposite to the first outside layer, when viewed from above or below in a vertical direction, and sets the detected area as a via possible area; and

a wiring information generating means for determining a

wiring pattern so that signal lines requiring tamper-resistance are wired only in the outside layer wiring possible areas and the via possible area, and generating wiring information that shows the determined wiring pattern.

8. The design apparatus of Claim 7 further comprising

an inside layer wiring setting means for referring to the component information, detecting an area where a first outside area wiring possible area of one outside layer overlaps another outside area wiring possible area of a second outside layer that is opposite to the first outside layer, when viewed from above or below in a vertical direction, and sets the detected area as an inside layer wiring possible area, wherein

the wiring information generating means determines the wiring pattern so that signal lines requiring tamper-resistance are wired only in the outside layer wiring possible areas, the via possible areas, and the inside layer wiring possible area, and generates the wiring information that shows the determined wiring pattern.

9. The design apparatus of Claim 8 further comprising

an opposite layer wiring setting means for referring to the component information and setting areas on one outside layer

covered by components as opposite layer wiring possible areas, wherein

the wiring information generating means determines the wiring pattern so that signal lines requiring tamper-resistance are wired in areas on another outside layer that is opposite to the outside layer, the areas on the other outside layer overlapping the opposite layer wiring possible areas when viewed from above or below in a vertical direction.

10. A design apparatus for a multilayer board, the design apparatus comprising:

a board information acquiring means for acquiring board information that shows (a) the number of layers and (b) ground/power-source layers;

a tamper-resistant signal line specifying means for specifying a signal line that requires tamper-resistance;

an inside layer wiring setting means for referring to the board information and setting layers sandwiched between two ground/power-source layers as wiring possible inside layers; and

a wiring information generating means for determining a wiring pattern so that signal lines requiring tamper-resistance are wired in the wiring possible inside layers, and generating

wiring information that shows the determined wiring pattern.

11. A design apparatus for a multilayer board, the design apparatus comprising:

a board information acquiring means for acquiring board information that shows (a) wiring of signal lines that require tamper-resistance and (b) positions of components connected to the signal lines;

an exposed portion detecting means for referring to the board information and detecting portions of the signal lines that are not covered by the components connected to the signal lines on outside layers; and

a placement information generating means for determining a placement pattern so that one or more components that have not been placed yet are placed to cover the detected portions, and generating placement information that shows the determined placement pattern.

12. The design apparatus of Claim 11 further comprising

an inside layer wiring detecting means for detecting portions of the signal lines wired on inside layers which are not sandwiched by the components on the outside layers when viewed from above or below in a vertical direction, wherein

the placement information generating means determines the placement pattern so that one or more components on one or more outside layers that have not been placed yet are placed to cover the portions detected by the inside layer wiring detecting means when viewed from above or below, and generates the placement information that shows the determined placement pattern.

13. The design apparatus of Claim 12 further comprising

an opposite layer exposed portion detecting means for referring to the board information and detecting portions of the signal lines that are wired on one outside layer and are not covered by components connected to the signal lines on another outside layer that is opposite to the outside layer, wherein

the placement information generating means determines the placement pattern so that one or more components on the opposite outside layer that have not been placed yet are placed to cover the portions detected by the opposite layer exposed portion detecting means when viewed from above or below, and generates the placement information that shows the determined placement pattern.

14. A design apparatus for a multilayer board, the design apparatus comprising:

a board information acquiring means for acquiring board information that shows (a) the number of layers and (b) wiring of signal lines;

a tamper-resistant signal line specifying means for specifying a signal line that requires tamper-resistance;

a plane layer detecting means for detecting, as plane layers, two layers that sandwich a layer on which the signal line is wired; and

a placement information generating means for determining a placement pattern so that sheets of foil on the plane layers cover the wiring of the signal line sandwiched by the plane layers when viewed from above or below in a vertical direction, and generating placement information that shows the determined placement pattern.

15. A design check apparatus for a multilayer board, the design check apparatus comprising:

a board information acquiring means for acquiring board information that shows (a) wiring of a signal line that requires tamper-resistance and (b) placement of components;

an exposed portion detecting means for referring to the board information and detecting portions of the signal line that are not covered by the components on outside layers; and

a warning means for outputting a warning indicating the portions detected by the exposed portion detecting means.

16. The design check apparatus of Claim 15 further comprising:

an inside layer uncovered portion detecting means for referring to the board information and detecting portions of the signal line in inside layers that are not sandwiched between components or sheets of foil placed on two outside layers when viewed from above or below in a vertical direction, wherein

the warning means further outputs a warning indicating the portions detected by the inside layer uncovered portion detecting means.

17. The design check apparatus of Claim 16 further comprising:

an opposite layer uncovered portion detecting means for referring to the board information and detecting portions of the signal line that are wired on one outside layer and are not covered by components on another outside layer that is opposite to the outside layer when viewed from above or below in a vertical direction, wherein

the warning means further outputs a warning indicating

the portions detected by the opposite layer uncovered portion detecting means.

18. A design method for a multilayer board, the design method comprising:

a component information acquiring step for acquiring component information that shows (a) positions of circuit components, (b) sizes of the components, and (c) terminals contained by the components;

a tamper-resistant signal line specifying step for specifying a signal line that requires tamper-resistance, among signal lines connecting terminals;

an outside layer wiring setting step for referring to the component information and setting areas on outside layers covered by circuit components as outside layer wiring possible areas;

a via setting step for referring to the component information, detecting an area where a first outside area wiring possible area of one outside layer overlaps another outside area wiring possible area of a second outside layer that is opposite to the first outside layer, when viewed from above or below in a vertical direction, and sets the detected area as a via possible area; and

a wiring information generating step for determining a

wiring pattern so that signal lines requiring tamper-resistance are wired only in the outside layer wiring possible areas and the via possible area, and generating wiring information that shows the determined wiring pattern.

19. A design method for a multilayer board, the design method comprising:

a board information acquiring step for acquiring board information that shows (a) the number of layers and (b) ground/power-source layers;

a tamper-resistant signal line specifying step for specifying a signal line that requires tamper-resistance;

an inside layer wiring setting step for referring to the board information and setting layers sandwiched between two ground/power-source layers as wiring possible inside layers; and

a wiring information generating step for determining a wiring pattern so that signal lines requiring tamper-resistance are wired in the wiring possible inside layers, and generating wiring information that shows the determined wiring pattern.

20. A design method for a multilayer board, the design method comprising:

a board information acquiring step for acquiring board information that shows (a) wiring of signal lines that require tamper-resistance and (b) positions of components connected to the signal lines;

an exposed portion detecting step for referring to the board information and detecting portions of the signal lines that are not covered by the components connected to the signal lines on outside layers; and

a placement information generating step for determining a placement pattern so that one or more components that have not been placed yet are placed to cover the detected portions, and generating placement information that shows the determined placement pattern.

21. A design method for a multilayer board, the design method comprising:

a board information acquiring step for acquiring board information that shows (a) the number of layers and (b) wiring of signal lines;

a tamper-resistant signal line specifying step for specifying a signal line that requires tamper-resistance;

a plane layer detecting step for detecting, as plane layers, two layers that sandwich a layer on which the signal line is

wired; and

a placement information generating step for determining a placement pattern so that sheets of foil on the plane layers cover the wiring of the signal line sandwiched by the plane layers when viewed from above or below in a vertical direction, and generating placement information that shows the determined placement pattern.

22. A design check method for a multilayer board, the design check method comprising:

a board information acquiring step for acquiring board information that shows (a) wiring of a signal line that requires tamper-resistance and (b) placement of components;

an exposed portion detecting step for referring to the board information and detecting portions of the signal line that are not covered by the components on outside layers; and

a warning step for outputting a warning indicating the portions detected by the exposed portion detecting step.

23. A program for allowing a computer to design a multilayer board, the program comprising:

a component information acquiring step for acquiring component information that shows (a) positions of circuit

components, (b) sizes of the components, and (c) terminals contained by the components;

a tamper-resistant signal line specifying step for specifying a signal line that requires tamper-resistance, among signal lines connecting terminals;

an outside layer wiring setting step for referring to the component information and setting areas on outside layers covered by circuit components as outside layer wiring possible areas;

a via setting step for referring to the component information, detecting an area where a first outside area wiring possible area of one outside layer overlaps another outside area wiring possible area of a second outside layer that is opposite to the first outside layer, when viewed from above or below in a vertical direction, and sets the detected area as a via possible area; and

a wiring information generating step for determining a wiring pattern so that signal lines requiring tamper-resistance are wired only in the outside layer wiring possible areas and the via possible area, and generating wiring information that shows the determined wiring pattern.

24. A program for allowing a computer to design a multilayer board, the program comprising:

a board information acquiring step for acquiring board information that shows (a) the number of layers and (b) ground/power-source layers;

a tamper-resistant signal line specifying step for specifying a signal line that requires tamper-resistance;

an inside layer wiring setting step for referring to the board information and setting layers sandwiched between two ground/power-source layers as wiring possible inside layers; and

a wiring information generating step for determining a wiring pattern so that signal lines requiring tamper-resistance are wired in the wiring possible inside layers, and generating wiring information that shows the determined wiring pattern.

25. A program for allowing a computer to design a multilayer board, the program comprising:

a board information acquiring step for acquiring board information that shows (a) wiring of signal lines that require tamper-resistance and (b) positions of components connected to the signal lines;

an exposed portion detecting step for referring to the board information and detecting portions of the signal lines that are not covered by the components connected to the signal

lines on outside layers; and

a placement information generating step for determining a placement pattern so that one or more components that have not been placed yet are placed to cover the detected portions, and generating placement information that shows the determined placement pattern.

26. A program for allowing a computer to design a multilayer board, the program comprising:

a board information acquiring step for acquiring board information that shows (a) the number of layers and (b) wiring of signal lines;

a tamper-resistant signal line specifying step for specifying a signal line that requires tamper-resistance;

a plane layer detecting step for detecting, as plane layers, two layers that sandwich a layer on which the signal line is wired; and

a placement information generating step for determining a placement pattern so that sheets of foil on the plane layers cover the wiring of the signal line sandwiched by the plane layers when viewed from above or below in a vertical direction, and generating placement information that shows the determined placement pattern.

27. A program for allowing a computer to check a design of a multilayer board, the program comprising:

a board information acquiring step for acquiring board information that shows (a) wiring of a signal line that requires tamper-resistance and (b) placement of components;

an exposed portion detecting step for referring to the board information and detecting portions of the signal line that are not covered by the components on outside layers; and

a warning step for outputting a warning indicating the portions detected by the exposed portion detecting step.

28. A recording medium recording a program for allowing a computer to design a multilayer board, the program comprising:

a component information acquiring step for acquiring component information that shows (a) positions of circuit components, (b) sizes of the components, and (c) terminals contained by the components;

a tamper-resistant signal line specifying step for specifying a signal line that requires tamper-resistance, among signal lines connecting terminals;

an outside layer wiring setting step for referring to the component information and setting areas on outside layers covered by circuit components as outside layer wiring possible areas;

a via setting step for referring to the component information, detecting an area where a first outside area wiring possible area of one outside layer overlaps another outside area wiring possible area of a second outside layer that is opposite to the first outside layer, when viewed from above or below in a vertical direction, and sets the detected area as a via possible area; and

a wiring information generating step for determining a wiring pattern so that signal lines requiring tamper-resistance are wired only in the outside layer wiring possible areas and the via possible area, and generating wiring information that shows the determined wiring pattern.

29. A recording medium recording a program for allowing a computer to design a multilayer board, the program comprising:

a board information acquiring step for acquiring board information that shows (a) wiring of signal lines that require tamper-resistance and (b) positions of components connected to the signal lines;

an exposed portion detecting step for referring to the board information and detecting portions of the signal lines that are not covered by the components connected to the signal lines on outside layers; and

a placement information generating step for determining a placement pattern so that one or more components that have not been placed yet are placed to cover the detected portions, and generating placement information that shows the determined placement pattern.